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the r123 in the air out on the business side, this is not, somehow, about guns and the second wave Aigo .Integrated circuit (IC) semiconductor fabrication is a complex process that involves many steps including, photolithography (exposing and developing a photoresist), a selective etch, photoresist removal, and wet or dry chemical cleaning of the surface. This process is repeated many times for the same wafer being processed. Each time a new processing step is performed the semiconductor surface is not clean, and each step creates more contaminants. Therefore, it is necessary to clean the IC device surface thoroughly after each processing step. Further, the need for increased device density has made it necessary to decrease the device size while having the same number of devices. This includes the lateral dimension and also the height of the device as well as decreasing the depth of the device. To achieve the necessary device feature size for some current semiconductor devices, the depth of various layers of the device needs to be very small. The smaller the width of a transistor gate electrode, the smaller the transistor gate electrode is, the more prone the transistor gate electrode becomes to damage. This is because there are more transverse electrical fields in the smaller transistor gate electrode that need to be screened by the gate dielectric and gate electrode material. Cleaning steps used for post etch residue removal are also deleterious for the gate dielectric or gate electrode material. Cleaning steps such as after a second spacer formation step, polymer removal, or resist stripping, perform very poorly in removing barrier layer materials that are used in gate stacks. Further, cleaning steps such as used after removing the patterning photoresist after ion implantation also cause problems with the barrier material. Therefore, for gate dielectric and gate electrode material, the processing steps that clean the material must be minimized or eliminated. Further, it is necessary to minimize the damage caused by cleaning steps, thereby allowing the processing to be kept to a minimum. An example of a conventional gate stack process to form a gate dielectric is as follows. A substrate is placed in a chamber which is fitted with a substrate holder. A gate dielectric material is deposited on the substrate surface. The gate dielectric material is formed by chemical vapor deposition (CVD) at relatively high temperatures (450-500 degrees centigrade) and also at relatively high pressures (between about 15 Torr to about 100 Torr) using a reactive gas such

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